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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/797,604	YI ET AL.
	Examiner	Art Unit
	Kevin Quinto	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-30 and 32-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-30 and 32-39* is/are allowed.

6)☒ Claim(s) *1-3,5,10 and 11* is/are rejected.

7)☒ Claim(s) *6-9 and 12-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *24 August 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 2, 3, 5-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 3, 5, 10, and 11 are rejected under 35 U.S.C. 102(a, b) as being anticipated by Ishida (JP 11-261056).

4. In reference to claim 1, Ishida (JP 11-261056) discloses a device which meets the claim. Figures 1-6 and 8-13 disclose two different semiconductor devices which each have a substrate (10: figures 1-6, 40: figures 8-13) and a gate electrode (32: figures 1-6, 62: figures 8-13) comprising of at least first and second elongate wirings which intersect at an intersection regions of the gate electrode (32, 62). A gate dielectric layer (28: figures 1-6, 58: figures 8-13) is interposed between the gate electrode (32, 62) and the surface of the substrate (10, 40). There is at least one oxide region (26: figures 1-6, 56: figures 8-13) located in the substrate (10, 40) below the

intersection region of the gate electrode (32, 62). The thickness of the oxide region (26, 56) is thicker than that of the gate dielectric layer (28, 58).

5. With regard to claim 2, the oxide region (26, 56) is a field oxide region.

6. In reference to claim 3, Ishida (JP 11-261056) discloses a similar device. Figures 1-6 and 8-13 disclose two different semiconductor devices which each illustrate a semiconductor device with a mesh-shaped gate electrode (32, 62) located over a surface of a substrate (10, 40). The mesh-shaped gate electrode (32, 62) has a plurality of openings aligned over respective source/drain regions (20, 22: figures 1-6, 64, 66: figures 8-13) of the substrate (10, 40). The mesh-shaped gate electrode (32, 62) comprises a plurality of first elongate wirings extending parallel to one another, and a plurality of second elongate wirings extending parallel to one another, and wherein the first elongate wirings intersect the second elongate wirings to define an array of gate intersection regions over the surface of the substrate (10, 40) and to further define an array of source/drain regions (20, 22, 64, 66) of the substrate (10, 40). A gate dielectric layer (28, 58) is interposed between the mesh-shaped gate electrode (32, 62) and the surface of the substrate (10, 40). At least one oxide region (26, 56) is located in the substrate (10, 40) below the mesh-shaped gate electrode (32, 62). A thickness of the oxide region (26, 56) is greater than that of the gate dielectric (28, 58).

7. With regard to claim 5, the at least one oxide region (26: figures 1-6, 56: figures 8-13) located in the substrate (10, 40) below the intersection region of the gate electrode (32, 62).

8. In reference to claim 10, the array of source/drain regions comprises a plurality of spaced apart alternating source and drain regions so that each drain region (22, 66) is surrounded by four source regions (20, 64) and each source region (20, 64) is surrounded by four drain regions (22, 66).

9. With regard to claim 11, the oxide region (26, 56) is a field oxide region.

Allowable Subject Matter

10. Claims 19-30 and 32-39 are allowed.

11. Claims 6-9 and 12-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a field effect transistor using a mesh type gate, a mesh type electrode for the source or drain formed over a first dielectric layer and another mesh type electrode for the source or drain formed over a second different dielectric layer.

Conclusion

13. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on August 24, 2005 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS**

MADE FINAL. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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